IN THE DRAWINGS

Figures 1 and 2a-2c have been designated by a legend --PRIOR ART--. An Appendix including both a replacement sheet and an annotated sheet showing changes is attached following page 7 of this paper.

REMARKS

Claims 1-20 are pending in the application.

Claims 1-20 are rejected.

Claims 1-6 and 9-16 are rejected under 35 U.S.C. 102(b).

Claims 1-10 are rejected under 35 U.S.C. 102(b).

Drawings

Figures 1 and 2a-2c have been designated by a legend --Prior Art--.

Claim Rejections – 35 U.S.C. § 102

Claims 1-6 and 9-16 are rejected under 35 U.S.C. 102(b) as being anticipated by Fukuda (U.S. Patent No. 6,127,729).

Applicants traverse this rejection. Fukuda does not teach or suggest the invention of claims 1-20 for the reasons set forth in detail below.

Claims 1-6 and 9-16 have been amended to recite that the respective chip pads, the respective test pads, and the respective chip pads and test pads being arranged at substantially uniform intervals. Fukuda does not teach either a semiconductor chip or a tape carrier package in which the respective chip pads, the respective test pads, and the respective chip pads and test pads are arranged at substantially uniform intervals.

In order for a prior art reference to anticipate a claim under 35 U.S.C. 102 (e), each and every element of the claimed invention must be identically shown in the reference. For the reasons set forth above, the Examiner has not made a prima facie case of anticipation.

Claims 1-20 are rejected under 35 U.S.C. 102(b) as being anticipated by Aiki, et al. (JP 2002-303653).

Applicants traverse this rejection. Aiki, et al. does not teach or suggest the invention of claims 1-20 for the reasons set forth in detail below.

Claims 1-20 have been amended to recite that the respective chip pads, the respective test pads, and the respective chip pads and test pads being arranged at substantially uniform intervals. Aiki, et al. does not teach either a semiconductor chip or a tape carrier package in which the respective chip pads, the respective test pads, and the respective chip pads and test pads are arranged at substantially uniform intervals.

Claims 3 and 13 have been amended to recite that the chip pads are arranged in rows adjacent the main circuit area of the semiconductor chip, that the test pads are located within the rows of chip pads, and that the number of rows is four. Aiki, et al. does not teach either a semiconductor chip or a tape carrier package in which the chip pads are arranged in rows adjacent the main circuit area of the semiconductor chip, that the test pads are located within the rows of chip pads, and that the number of rows is four. Aiki, et al. describes no more than two rows of chip pads/test pads.

In order for a prior art reference to anticipate a claim under 35 U.S.C. 102 (e), each and every element of the claimed invention must be identically shown in the reference. For the reasons set forth above, the Examiner has not made a prima facie case of anticipation.

For the foregoing reasons, reconsideration and allowance of claims 1-20 of the application as amended is solicited. The Examiner is encouraged to telephone the undersigned at (503) 222-3613 if it appears that an interview would be helpful in advancing the case.

Respectfully submitted,

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I hereby certify that this correspondence is being transmitted to the U.S. Patent and Trademark Office via facsimile number (571) 273-8300 on January 3, 2006.

Stormi R. Davis

Dong-Han KIM

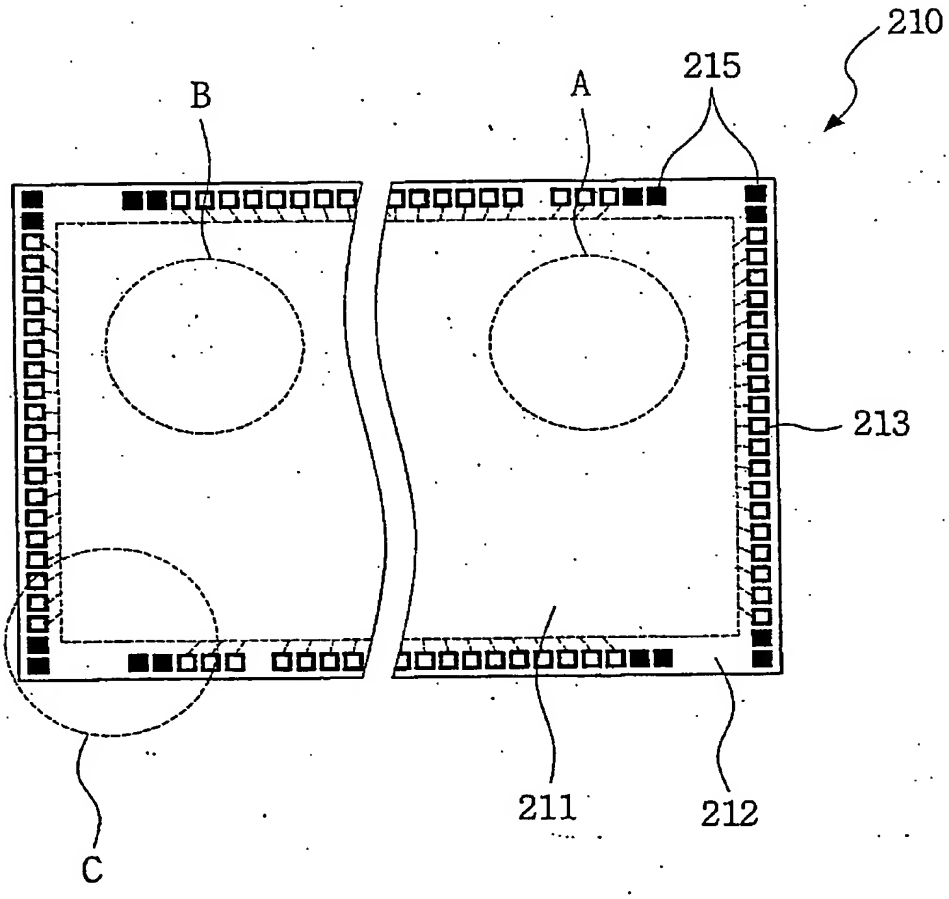
SEMICONDUCTOR CHIP WITH TEST PADS AND TAPE CARRIER PACKAGE USING THE SAME

Attorney Docket No. 9903-075/Application No. 10/801,501

Annotated Sheet Showing Changes

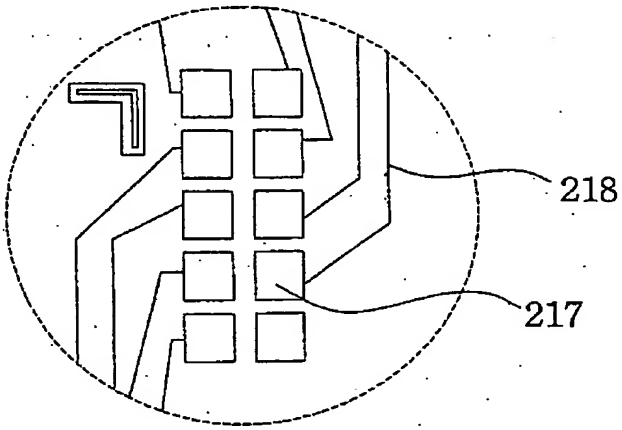
FIG. 1

(Prior ~~Conventional~~ Art)

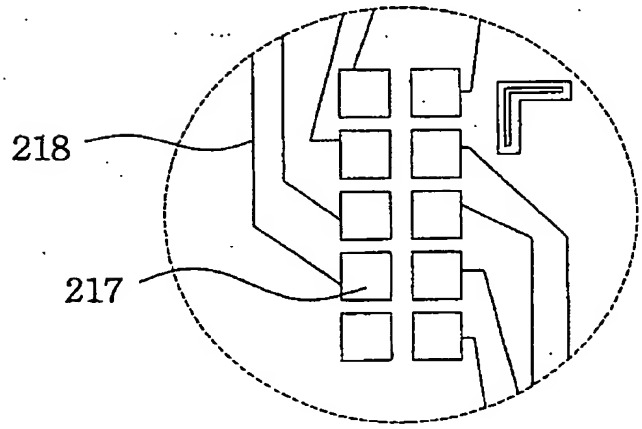


Dong-Han KIM
SEMICONDUCTOR CHIP WITH TEST PADS AND TAPE CARRIER PACKAGE USING THE SAME
Attorney Docket No. 9903-075/Application No. 10/801,501
Annotated Sheet Showing Changes

Prior FIG. 2a
(~~Conventional~~ Art)



Prior FIG. 2b
(~~Conventional~~ Art)



Prior FIG. 2c
(~~Conventional~~ Art)